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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/774,095	02/06/2004	Ole Agesen	A40	8377

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VMware, Inc.
ATTN: Darryl Smith
3145 Porter Drive
Palo Alto, CA 94304

EXAMINER	
KIM, DANIEL Y	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 04/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/774,095	AGESEN ET AL.	
	Examiner	Art Unit	
	Daniel Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-7, 26-28, 30-34, 36-38 and 40-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Killian (US Patent No. 5,479,630) and Moran et al (US Patent No. 6,738,869).

For claim 1, Killian discloses a computer system in which a virtual memory system is implemented, the computer system comprising a plurality of virtual memory pages, some of which being backed by a set of one or more physical memory pages and others of which being backed by a secondary memory, the computer system further comprising a primary data store containing a primary data item and a derived data store containing a derived data item, the primary data item and the derived data item each providing memory mapping information about a first virtual memory page, the derived data item being derived from the primary data item (a hybrid cache memory system includes primary cache and secondary cache which are not of the same physical-cache/virtual-cache characteristics, the primary cache has the physical cache characteristic of a physical tag and the virtual cache characteristic of a virtual index, the secondary cache has the physical-cache characteristics of a physical tag and a physical

index, and the secondary cache has a primary index segment used to derive an index to primary cache when tracing back from secondary cache, col. 3, lines 8-18).

Killian fails to disclose the remaining claim limitations.

Moran, however, discloses an actor, the actor modifying the primary data item in the primary data store so that the derived data item in the derived data store is incoherent with the primary data item (one or more processors may modify its own copy of a memory portion data such that incoherent or unmatched copies of the memory portion data exist within the system, col. 3, line 67, col. 4, lines 1-3)

a producer, the producer providing a first information indicating that the primary data item in the primary data store has been modified (one processor, the producer, is generating data and when completed writing all the data, updates a flag which indicates to other processors that the data is now ready to be used for further calculations or updates, col. 4, lines 28-32); and

a consumer, wherein the consumer receives the first information provided by the producer and, on occurrence of a coherency event at which the derived data item is not to be incoherent with the primary data item, the consumer eliminates the incoherency between the derived data item and the primary data item (a next user, the consumer, must wait until an update is complete, and after the producer is finished with all updates, the consumer can then proceed with data modified with the appropriate changes, col. 4, lines 35-39).

Killian and Moran are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been

obvious to a person of ordinary skill in the art at the time of the invention to include an actor which describes creating an incoherency because any copy of an updated and correct memory portion existing somewhere within the system has the danger of being erroneously overwritten or superceded by older, outdated and erroneous memory portion (col. 1, lines 31-34), as taught by Moran.

Likewise, it would have been obvious to include a producer and consumer because the producer/consumer model is a standard usage model to discuss coherency and ordering (col. 4, lines 25-26), as taught by Moran.

For claim 2, the combined teachings of Killian and Moran disclose the invention as per rejection of claim 1 above.

Killian further helps disclose the producer also provides a second information indicating a derived value based on the modification that has been made to the primary data item and a third information that can be used to determine whether the second information remains valid, and the consumer uses the second information to modify the derived data item to make the derived data item coherent with the primary data item if the third information indicates that the second information is valid (primary-cache blocks which may correspond to a block of a secondary-cache block are inspected when secondary cache block status or contents are to be changed, for each primary-cache block which is a subset of such secondary-cache block, such primary-cache block is invalidated, and whenever a block is to be loaded into secondary cache, the primary index segment of the prior contents is used to identify any corresponding blocks in the primary cache, which are also invalidated, col. 4, lines 37-46; the secondary cache has

a primary index segment, used to derive an index to primary cache when tracing back from secondary cache, col. 3, lines 16-18).

Claim 3 is rejected using the same rationale as for the rejection of claim 2 above.

For claim 4, the combined teachings of Killian and Moran disclose the invention as per rejection of claim 2 above.

Killian further helps disclose on occurrence of the coherency event, if the third information indicates that the second information is no longer valid, the consumer determines a current value for the primary data item in the primary data store and uses this current value for the primary data item to modify the derived data item in the derived data store to make the derived data item coherent with the primary data item (the primary cache is loaded with a block of words being a subset of the source secondary-cache block, and if the primary index segment does not match, the primary cache data at the first offset is flushed back to secondary cache and the stored primary index segment is replaced with the reference segment derived from the accessing virtual address, and the primary cache is loaded with a subset of the source secondary-cache block, col. 4, lines 21-32).

Claim 5 is rejected using the same rationale as for the rejection of claim 2 above.

Claim 6 is rejected using the same rationale as for the rejection of claim 1 above.

For claim 7, the combined teachings of Killian and Moran disclose the invention as per rejection of claim 1 above.

Killian further helps disclose the coherency event comprises encountering a computer instruction that invalidates an entry within a Translation Lookaside Buffer (the

virtual address is input to a translation look-aside buffer, where it is translated into a physical address, which is then parsed to form an index into the cache to address the appropriate cache location, and the tag for such location then is compared with another parse of the translated physical address, col. 2, lines 3-9).

Claim 26 is rejected using the same rationale as for the rejection of claim 1 above.

Claim 27 is rejected using the same rationale as for the rejection of claim 1 above.

Claim 28 is rejected using the same rationale as for the rejections of claim 2 above.

Claim 30 is rejected using the same rationale as for the rejection of claim 1 above.

Claim 31 is rejected using the same rationale as for the rejection of claim 3 above.

Claim 32 is rejected using the same rationale as for the rejection of claim 4 above.

Claim 33 is rejected using the same rationale as for the rejection of claim 4 above.

Claim 34 is rejected using the same rationale as for the rejection of claim 4 above.

Claim 36 is rejected using the same rationale as for the rejection of claim 1 above.

Claim 37 is rejected using the same rationale as for the rejection of claim 1 above.

Claim 38 is rejected using the same rationale as for the rejection of claim 1 above.

Claim 40 is rejected using the same rationale as for the rejection of claim 1 above.

Claim 41 is rejected using the same rationale as for the rejection of claim 2 above.

3. Claims 8 and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Killian (US Patent No. 5,479,630), Moran et al (US Patent No. 6,738,869) and Devine et al (US Patent No. 6,397,242).

For claim 8, the combined teachings of Killian and Moran disclose the invention as per rejection of claim 1 above.

These teachings fail to disclose the limitations of claim 8.

Devine, however, discloses the coherency event comprises a situation in which a Translation Lookaside Buffer is flushed (at explicit points, entries are flushed from the translation-lookaside buffer, col. 11, lines 65-67).

Killian, Moran and Devine are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include flushing a translation look-aside buffer because these are the explicit points at which

memory traces on page table pages can guarantee the coherency of a shadow copy (col. 11, lines 62-65), as taught by Devine.

For claim 16, the combined teachings of Killian and Moran disclose the invention as per rejection of claim 1 above.

These teachings fail to disclose the limitations of claim 16.

Devine, however, helps disclose virtualization software for supporting a virtual machine, wherein the primary data store comprises a guest operating system page table containing translations from virtual memory pages to guest physical pages and the derived data store comprises a shadow page table containing translations from virtual memory pages to hardware physical pages (memory traces keep the shadow page tables synchronized with virtual machine page tables, col. 11, line 67, col. 12, line 1).

Killian, Moran and Devine are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include guest page tables and shadow page tables because segmented architectures rely on descriptor tables stored in memory, and virtualization prevents processors from using directly the virtual machine segment descriptor tables, which forces the processors to keep second, shadow copies of the tables (col. 11, lines 51-56), and keeping shadow page tables synchronized with virtual machine page tables can lead to performance benefits (col. 11, line 67, col. 12, lines 1-2), as taught by Devine.

For claim 17, the combined teachings of Killian, Moran and Devine disclose the invention as per rejection of claim 16 above.

Devine further helps disclose the modification to the primary data item triggers a write trace that has been placed on the primary data store, and the producer provides the first information in response to the triggering of the write trace (a write-trace on any given physical page of the virtual machine to be notified of all write accesses made to that page in a transparent manner, col. 11, lines 22-24).

For claim 18, the combined teachings of Killian, Moran and Devine disclose the invention as per rejection of claim 16 above.

Devine further helps disclose the computer system comprises a plurality of physical processors and the virtual machine comprises a plurality of virtual processors, wherein a first virtual processor is the producer and a second virtual processor is the consumer (the invention may also be used for virtualizing systems that have a plurality of hardware processors, in which case the invention further comprises a plurality of virtual processors included in the virtual machine and virtual machine monitor descriptor tables for each virtual processor, col. 7, lines 18-22).

4. Claims 9-15, 29, 35 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Killian (US Patent No. 5,479,630), Moran et al (US Patent No. 6,738,869) and James et al (US Patent No. 6,421,745).

For claim 9, the combined teachings of Killian and Moran disclose the invention as per rejection of claim 1 above.

These teachings fail to disclose the limitations of claim 9.

James, however, discloses a patch channel that is used by the producer to communicate the first information to the consumer (frames of data are transmitted from a producer device to a consumer device over a data bus, col. 3, lines 62-64).

Killian, Moran and James are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a patch channel because this would allow transmission of data between producers and consumers (col. 3, lines 62-64) as taught by James.

For claim 10, the combined teachings of Killian, Moran and James disclose the invention as per rejection of claim 9 above.

James further helps disclose the producer can write to the patch channel at the same time that the consumer reads from the patch channel, without any data races (each port within a plug allows duplex communications with a connected node, through the data port the computer, acting as producer, can send data to an instrument, acting as consumer, and can also receive data as a consumer device from the instrument, acting as a producer device, col. 2, lines 58-63).

Claim 11 is rejected using the same rationale as for the rejection of claim 10 above.

For claim 12, the combined teachings of Killian and Moran disclose the invention as per rejection of claim 9 above.

These teachings fail to disclose the limitations of claim 12.

James, however, helps disclose the patch channel comprises a half-duplex communication channel that is used exclusively by the producer and the consumer (page tables at a consumer device and the corresponding page table entries programmed at a producer device can be utilized for transfers of data from a producer device to a consumer device through any appropriate plug, including simplex, duplex and dual duplex plugs, col. 12, lines 1-6).

For claim 13, the combined teachings of Killian, Moran and James disclose the invention as per rejection of claim 12 above.

James further helps disclose the patch channel also comprises a set data structure stored in memory that is shared by the producer and the consumer (for the transfer of large frames of data, the consumer device programs an array of page table entries into a control register of the producer device, col. 4, lines 1-3).

Claim 14 is rejected using the same rationale as for the rejection of claim 13 above.

For claim 15, the combined teachings of Killian, Moran and James disclose the invention as per rejection of claim 9 above.

James further helps disclose additional producers and additional consumers, and wherein the patch channel is one of a plurality of patch channels in a patch channel matrix, wherein each patch channel in the patch channel matrix is used by a different pair consisting of a single producer and a single consumer (the connections are virtual representations of data flows between computers and instruments, col. 2, lines 40-42; fig. 2, items 24-36).

Claim 29 is rejected using the same rationale as for the rejections of claims 1 and 12 above.

Claim 35 is rejected using the same rationale as for the rejections of claims 10 and 11 above.

Claim 42 is rejected using the same rationale as for the rejection of claims 9-10 above.

5. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Killian (US Patent No. 5,479,630), Moran et al (US Patent No. 6,738,869), Devine et al (US Patent No. 6,397,242) and James et al (US Patent No. 6,421,745).

For claim 19, the combined teachings Killian, Moran and Devine disclose the invention as per rejection of claim 16 above.

These teachings fail to disclose the limitations of claim 19.

James however, helps disclose a plurality of physical processors and the virtual machine comprises a plurality of virtual processors, wherein a first virtual processor is both the producer and the consumer (a computer acting as a producer can send data, and can also receive data as a consumer, col. 2, lines 60-63, fig. 2, items 24-36).

Killian, Moran, Devine and James are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a virtual processor to be both a producer and consumer because this would allow for

duplex communications between connected nodes (col. 2, lines 58-67), as taught by James.

6. Claims 20-25, 39 and 43-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Killian (US Patent No. 5,479,630), Moran et al (US Patent No. 6,738,869), Devine et al (US Patent No. 6,397,242), James et al (US Patent No. 6,421,745), Agesen et al (US Patent No. 6,961,806) and Uhlig et al (US PGPub No. 20040117593).

For claim 20, the combined teachings of Killian, Moran, Devine and James disclose the invention as per rejection of claim 19 above.

These teachings fail to disclose the limitations of claim 20.

Agesen, however, helps disclose these limitations through the following:

a computer system includes at least one virtual machine, a plurality of virtual processors all running on an underlying hardware platform and a software interface layer that establishes traces on primary structures located in a common memory space as needed for the different virtual processors (abstract), and a virtual operating system (col. 2, lines 48-53),

one cached entry in the VMM descriptor tables for each segment of the processor, the binary translation sub-system selectively accessing each cached entry instead of the corresponding shadow entry (col. 5, lines 61-64), and

VMM descriptor tables, including shadow descriptors, that correspond to predetermined ones of the VM descriptor tables, and the VMM also includes a segment

tracking sub-system/module that compares the shadow descriptors with their corresponding VM segment descriptors, and indicates any lack of correspondence between shadow descriptor tables with the corresponding VM descriptor tables, and updates the shadow descriptors so that they correspond to their respective corresponding VM segment descriptors (col. 5, lines 50-59).

Uhlig also helps disclose these limitations through the following:

a modification of content of an active address translation data structure and modifying an entry in the active address translation data structure to conform to a corresponding entry in a guest address translation data structure (abstract),

guest address translation data structure is managed by the guest OS, which can access and modify any entry in the guest translation data structure, some entries of which include fields that are specifically designated for operational use by software (par. 0023), and

the VMM modifies the active address translation data structure upon receiving control over an event initiated by guest software and determining that the likely cause of the event is an inconsistency between the content of the active address translation data structure and the content of the guest address translation data structure (par. 0025).

Killian, Moran, Devine, James, Agesen and Uhlig are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a virtual computer system with physical hardware, virtualization software for a virtual machine, guest operating system and interactions between these

elements and guest OS page tables and shadow page tables because this would provide a system and method of operation that allows for the generalization of traces and the implementation of multiprocessor virtual machine monitors (col. 8, lines 41-44), as taught by Agesen.

Claim 21 is rejected using the same rationale as for the rejections of claims 2 and 20 above.

Claim 22 is rejected using the same rationale as for the rejections of claims 9-12 and 20 above.

Claim 23 is rejected using the same rationale as for the rejections of claims 15-16 and 20 above.

Claim 24 is rejected using the same rationale as for the rejections of claims 15 and 23 above.

Claim 25 is rejected using the same rationale as for the rejection of claim 20 above.

Claim 39 is rejected using the same rationale as for the rejections of claims 19 and 20 above.

Claim 43 is rejected using the same rationale as for the rejections of claims 1, 15 and 20 above.

Claim 44 is rejected using the same rationale as for the rejections of claims 2 and 43 above.

Claim 45 is rejected using the same rationale as for the rejections of claims 9-12 and 43 above.

Claim 46 is rejected using the same rationale as for the rejection of claim 43 above.

Claim 47 is rejected using the same rationale as for the rejections of claims 43 above.

Citation of Pertinent Prior Art

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Arimilli et al (US Patent No. 6,658,538) discloses producer processors process and store or modify large amounts of data in a set of memory pages.

Turner (US Patent No. 6,212,612) discloses a system and method for multi-channel data management with dynamically configurable routing, half- and full-duplex data communications channels through crossbar access ports, and allocation of pages to producers of data, and reception by consumers.

Van Doren et al (US Patent No. 7,000,080) discloses a channel-based mechanism resolves race conditions in a computer system between a first processor writing modified data back to memory and a second processor trying to obtain a copy of the modified data.

Contact Information

8. Any inquiries concerning this action or earlier actions from the examiner should be directed to Daniel Kim, reachable at 571-272-2742, on Mon-Fri from 8:30am-5pm. If

attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan, is also reachable at 571-272-4210.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information from published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. All questions regarding access to the Private PAIR system should be directed to the Electronic Business Center (EBC), reachable at 866-217-9197.

DK

4-20-06

PIERRE VITAL
PRIMARY EXAMINER